Department of Electrical Engineering
Govt. Polytechnic,Nuapda, Odisha Pin- 766105

LABORATORYMANUAL

Digital Electronics & Microprocessor Lab

(5th Semester)

Prepared By: **Udaya Meher Lect.in ETC**

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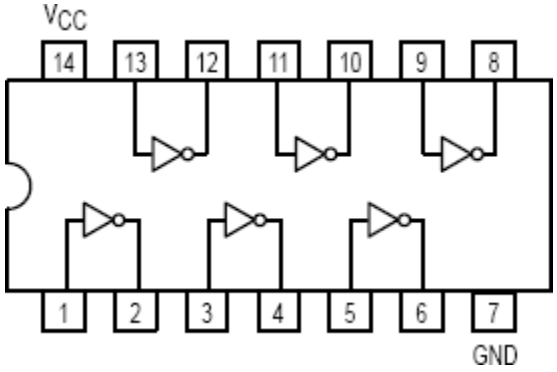
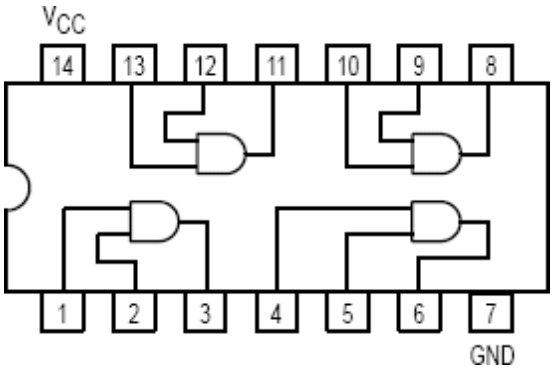
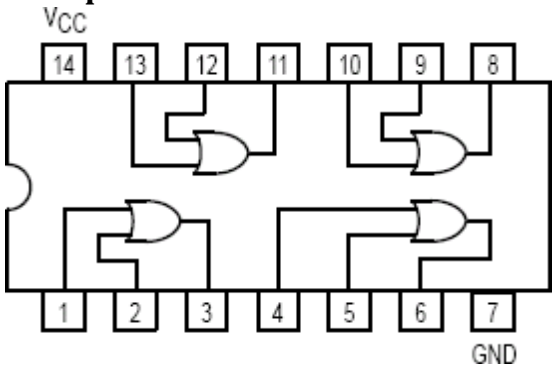
Inverter Gate (NOT Gate) 7404LS



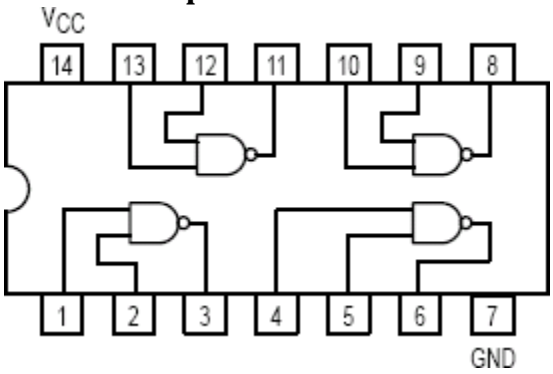
2-Input AND Gate 7408LS



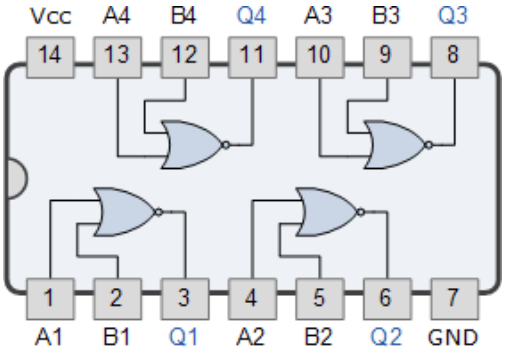
2-Input OR Gate 7432LS



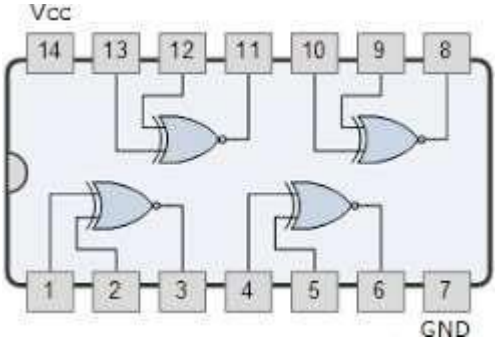
2-Input NAND Gate 7400LS



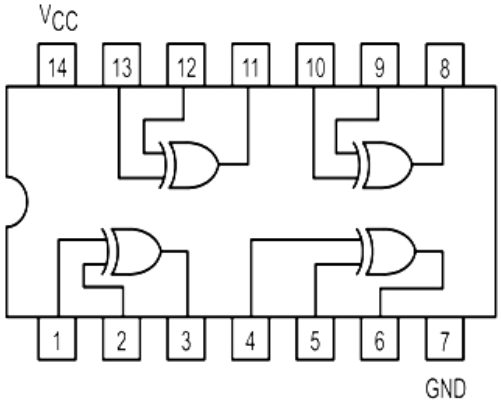
2-Input NOR Gate 7402LS



2-Input XNOR Gate 74266LS



2-Input XOR Gate 7486LS



Experiment No:1 Date:____/_/_____

Aim: - To Verify truth tables of AND, OR, NOT, NOR, NAND, XOR, XNOR gates.

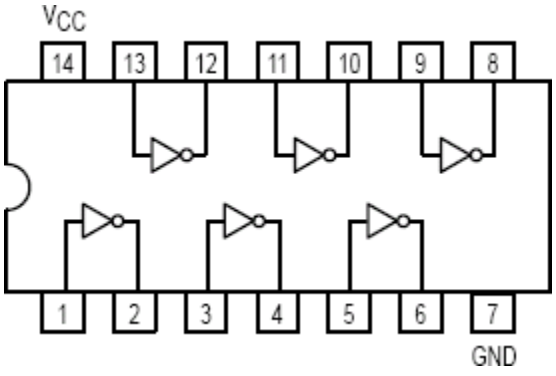
Apparatus Required: -

1. All the basic gates mention in the fig**.**
2. IC Trainer Kit

Procedure: -

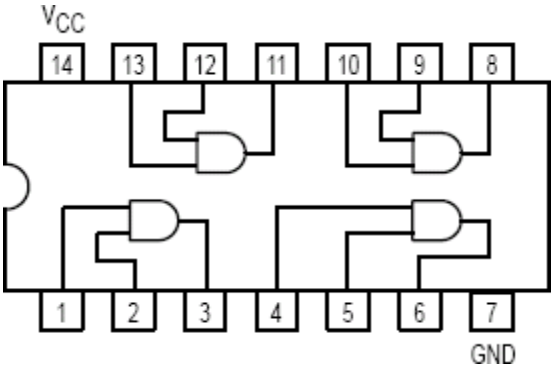
1. Place the IC on IC Trainer Kit.
2. Connect V_{CC} and ground to respective pins of IC Trainer Kit.
3. Connect the inputs to the input switches provided in the IC Trainer Kit.
4. Connect the outputs to the switches of O/P LEDs,
5. Apply various combinations of inputs according to the truth table and observe condition of LEDs.
6. Disconnect output from the LEDs and note down the corresponding multimeter voltage readings for various combinations of inputs**.**

Inverter Gate (NOT Gate) 7404LS



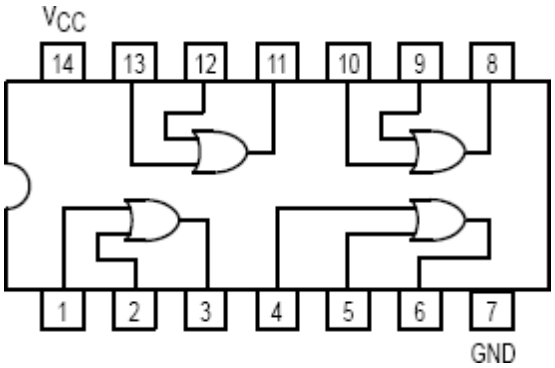
A	O/P
0	1
1	0

2-Input AND Gate 7408LS



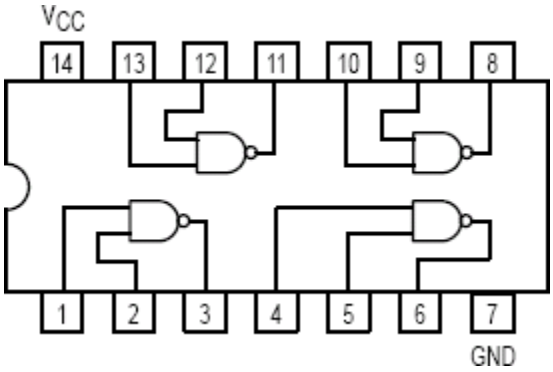
A	B	O/P
0	0	0
0	1	0
1	0	0
1	1	1

2-Input OR Gate 7432LS



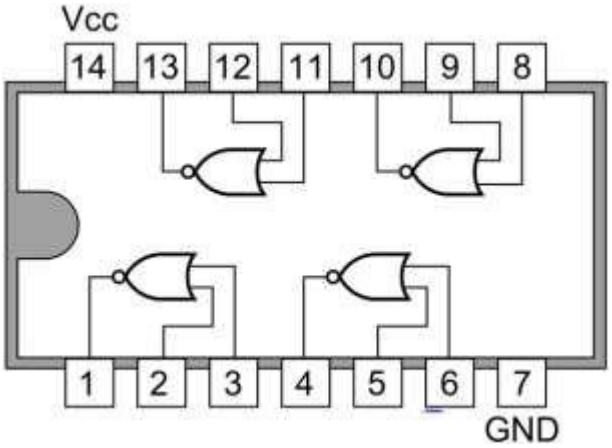
A	B	O/P
0	0	0
0	1	1
1	0	1
1	1	1

2-Input NAND Gate 7400LS



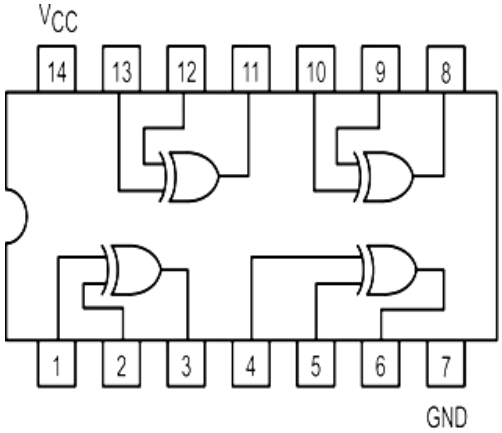
A	B	O/P
0	0	1
0	1	1
1	0	1
1	1	0

2-Input NOR Gate 7402LS



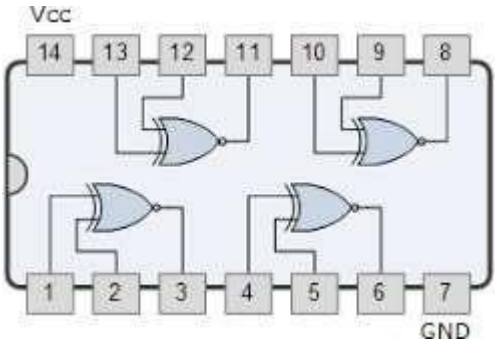
A	B	O/P
0	0	1
0	1	0
1	0	0
1	1	0

2-Input XOR Gate 7486LS



A	B	O/P
0	0	0
0	1	1
1	0	1
1	1	0

2-Input XNOR Gate 74266LS



A	B	O/P
0	0	1
0	1	0
1	0	0
1	1	1

Conclusion:-

Truth table of logic gates are verified.

Experiment No:2 **Date:___/_/_____**

Aim: - Implementation of various gates by using universal properties of NAND & NOR gatesand Verify truth table.

APPARATUS REQUIRED

1. Digital IC trainer kit
2. IC 7400 (NAND gate)
3. IC 7402(NOR gate)

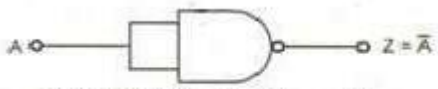
THEORY:

NAND OR NOR gates are sufficient for the realization of any logic expression. because ofthis reason, NAND and NOR gates are known as UNIVERSAL gates.

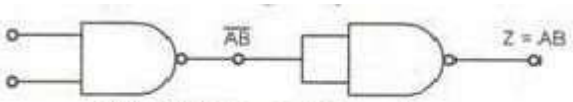
1. For NAND gate as universal gate

PROCEDURE:

1. Make the connections as per the logic diagram.
2. Connect +5v to pin 14 & ground to pin 7 of IC 7400
3. Apply diff combinations of inputs to the i/p terminals.
4. Note o/p for NAND as universal gate.
5. Verify the truth table.



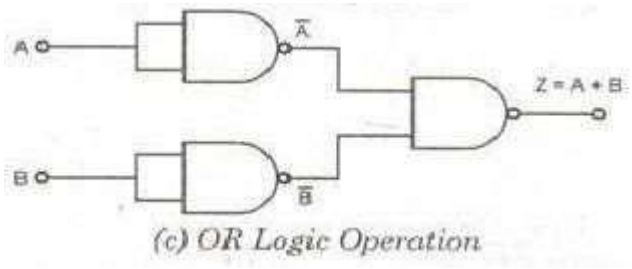
(a) NOT Logic Operation



(b) AND Logic Operation

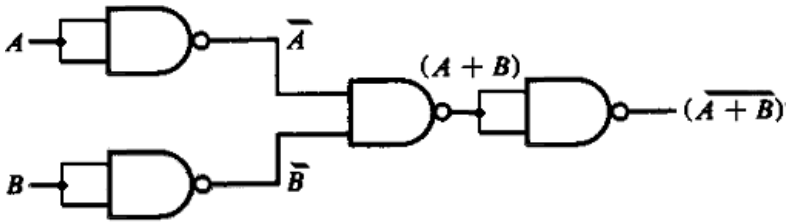
A	Ā
0	1
1	0

A	B	AB
0	0	0
0	1	0
1	0	0
1	1	1



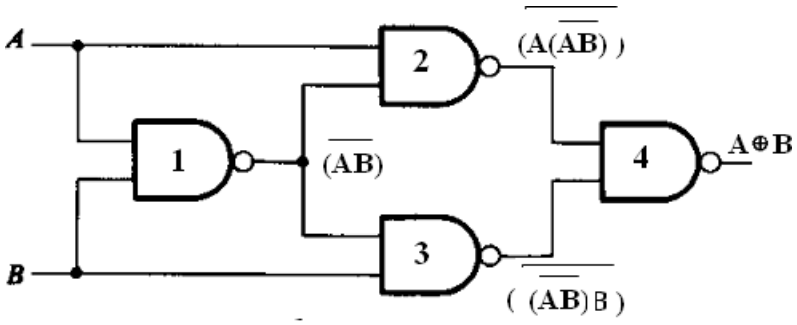
(c) OR Logic Operation

A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1



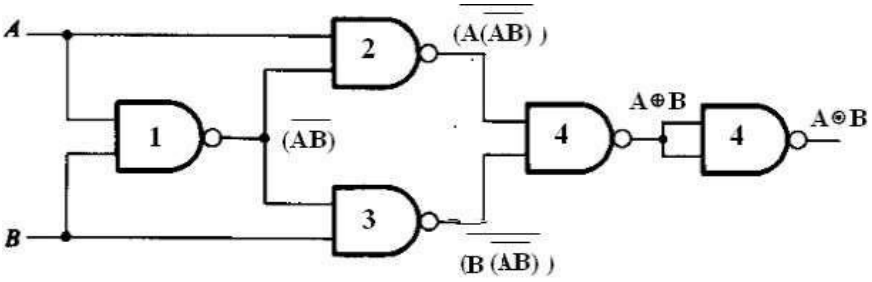
NOR Logic operation

A	*B*	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0



XOR Logic operation

A	B	A⊕B
0	0	0
0	1	1
1	0	1
1	1	0



XNOR Logic operation

A	B	A⊙B
0	0	1
0	1	0
1	0	0
1	1	1

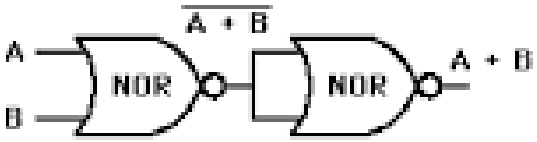
2.For NOR gate as universal gate

PROCEDURE:

1. Make the connections as per the logic diagram.
2. Connect +5v to pin 14 & ground to pin 7 of IC 7402
3. Apply diff combinations of inputs to the i/p terminals.
4. Note o/p for NAND as universal gate.
5. Verify the truth table

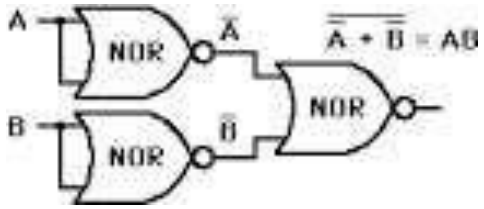
NOT Logic operation

A	$\bar{A}$
0	1
1	0



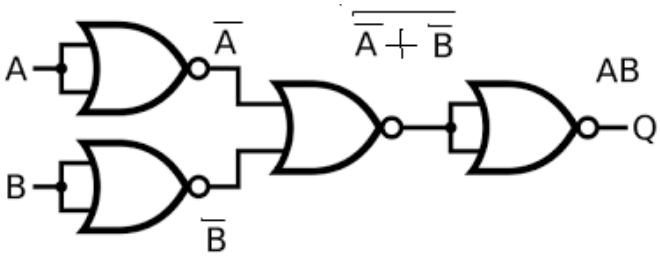
OR Logic operation

A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1



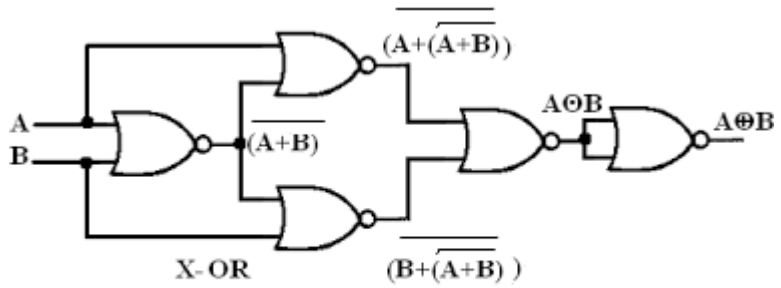
AND Logic operation

A	B	AB
0	0	0
0	1	0
1	0	0
1	1	1



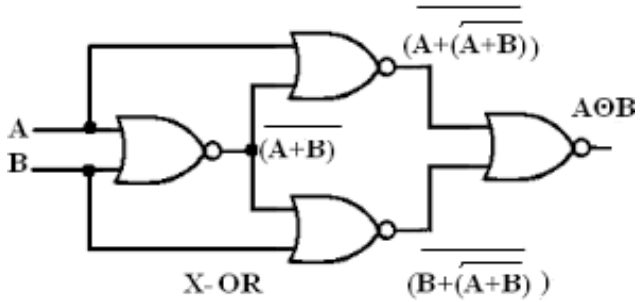
NAND Logic operation

A	B	AB
0	0	1
0	1	1
1	0	1
1	1	0



XOR Logic operation

A	B	A⊕B
0	0	0
0	1	1
1	0	1
1	1	0



A	B	AΘB
0	0	1
0	1	0
1	0	0
1	1	1

Conclusion:-

We have constructed and verified truth table of all gates using universal gates NAND and NOR gate.

Experiment No:3 **Date:___/_/_____**

Aim: - Implementation of half adder and Full adder using logic gates.

APPARATUS REQUIRED

1.IC 7486, IC 7432, IC 7408, IC 7400.
2. Digital trainer kit.

THEORY:

Half-Adder: A combinational logic circuit that performs the addition of two data bits, A and B, is called a half-adder. Addition will result in two output bits; one of which is the sum bit, S, and the other is the carry bit, C. The Boolean functions describing the half-adder are:

$S = A \oplus B$ $C = A\,B$

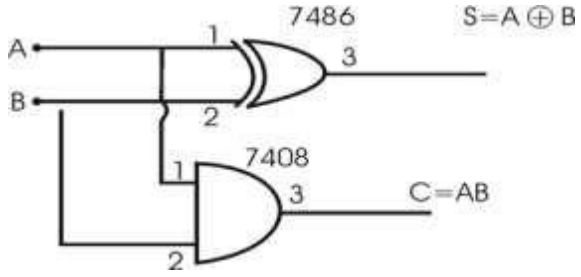
Full-Adder: The half-adder does not take the carry bit from its previous stage into account. This carry bit from its previous stage is called carry-in bit. A combinational logic circuit that adds two data bits, A and B, and a carry-in bit, Cin, is called a full-adder. The Boolean functions describing the full-adder are:

$S = (x \oplus y) \oplus C_{in}$ $C = xy + C_{in}(x \oplus y)$

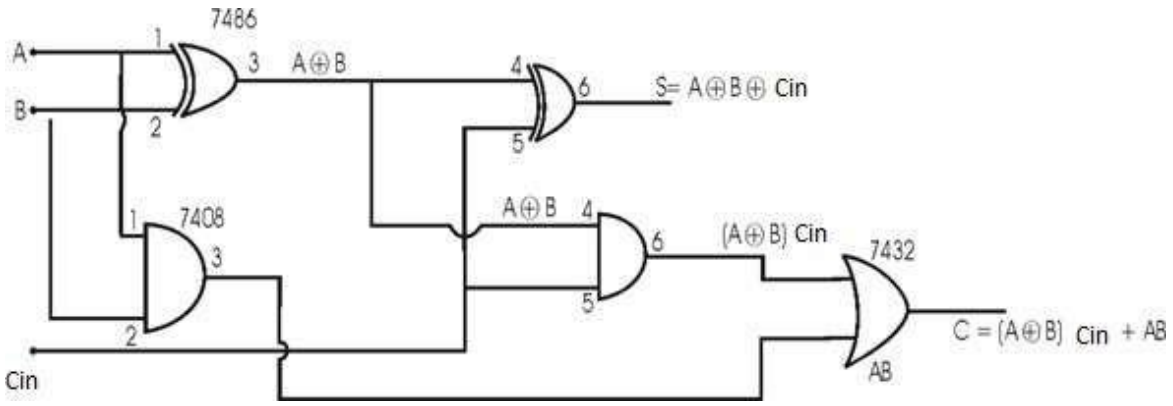
Procedure: -

1. Verify the gates.
2. Make the connections as per the circuit diagram.
3. Switch on V_{CC} and apply various combinations of input according to the truth table.
4. Note down the output readings for half and full adder sum and the carry bit for different combinations of inputs.

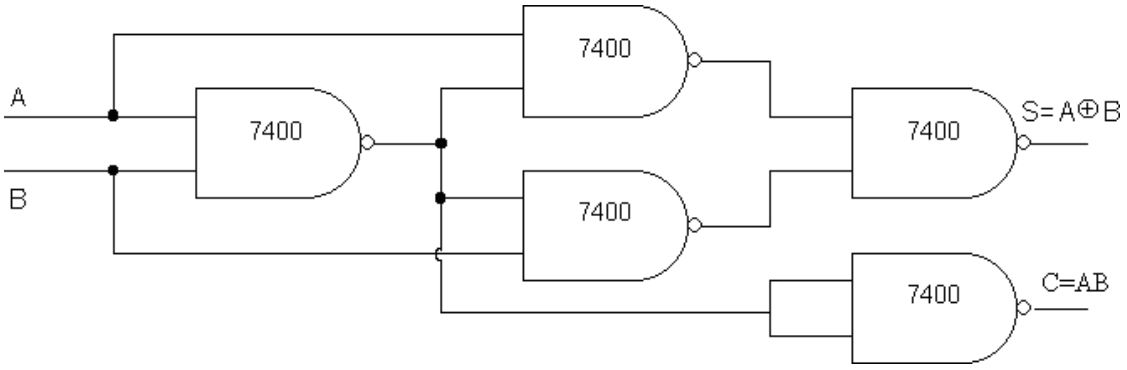
Half Adder using basic gates:-



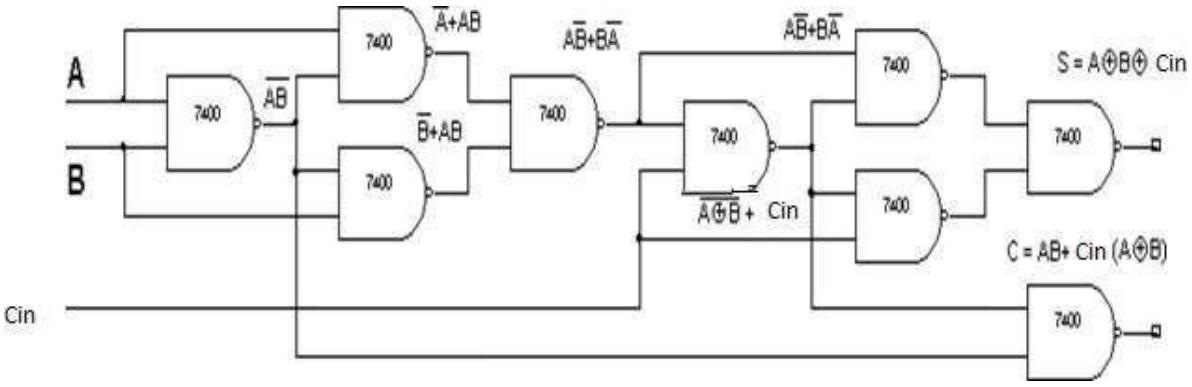
Full Adder using basic gates:-



Half Adder using NAND gates only:-

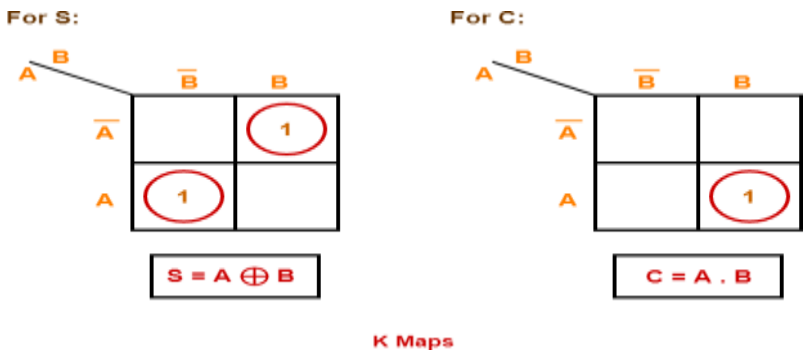


Full Adder using NAND gates only:-



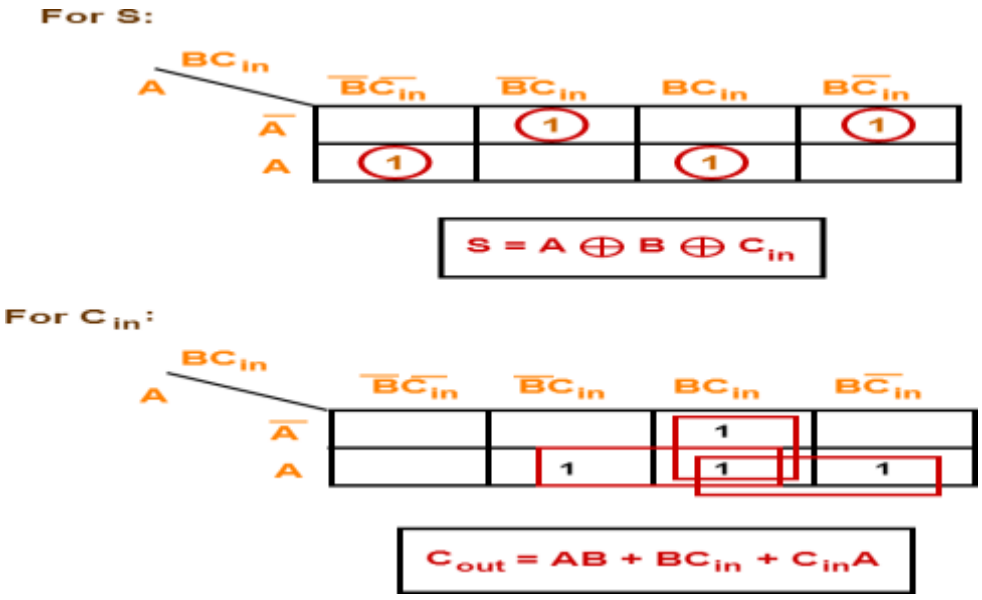
K-map for half adder

Half adder			
A	**B**	**S**	**C**
0	0		
0	1		
1	0		
1	1		



K-map for full adder

Full Adder				
A	**B**	Cin	**S**	**C**
0	**0**	**0**		
0	**0**	**1**		
0	**1**	**0**		
0	**1**	**1**		
1	**0**	**0**		
1	**0**	**1**		
1	**1**	**0**		
1	**1**	**1**		



Conclusion: -

Half adder and full adder are constructed and their truth tables are verified.

Experiment No:4 **Date:___/_/_**

Aim: - Implementation of half subtractor and Full subtractor using logic gates.

APPARATUS REQUIRED

1.IC 7486, IC 7432, IC 7408,IC7404, IC7400.
2. Digital trainer kit.

THEORY:

Half Subtractor: Subtracting a single-bit binary value B from another A (i.e. A -B) produces a difference bit D and a borrow out bit B-out. This operation is called half subtraction and the circuit to realize it is called a half subtractor. The Boolean functions describing the halfSubtractor are:

$$D = A \oplus B \qquad B_r = \overline{A}\, B$$

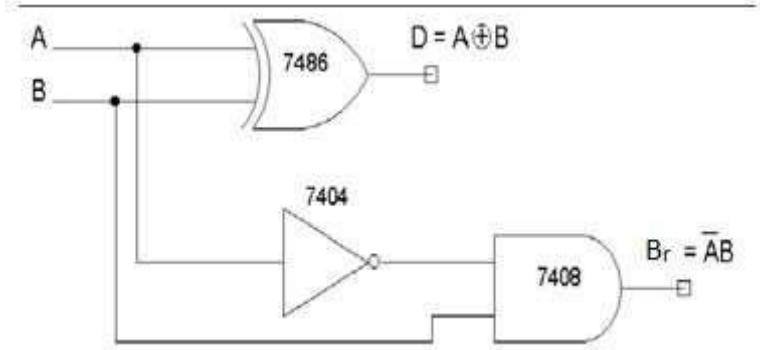
Full Subtractor: Subtracting two single-bit binary values, B, Cin from a single-bit value A produces a difference bit D and a borrow out Br bit. This is called full subtraction. The Boolean functions describing the full-subtracter are:

$$D = (x \oplus y) \oplus B_{in} \qquad B_r = \overline{A}B + \overline{A}\,(B_{in}) + B\,(B_{in})$$

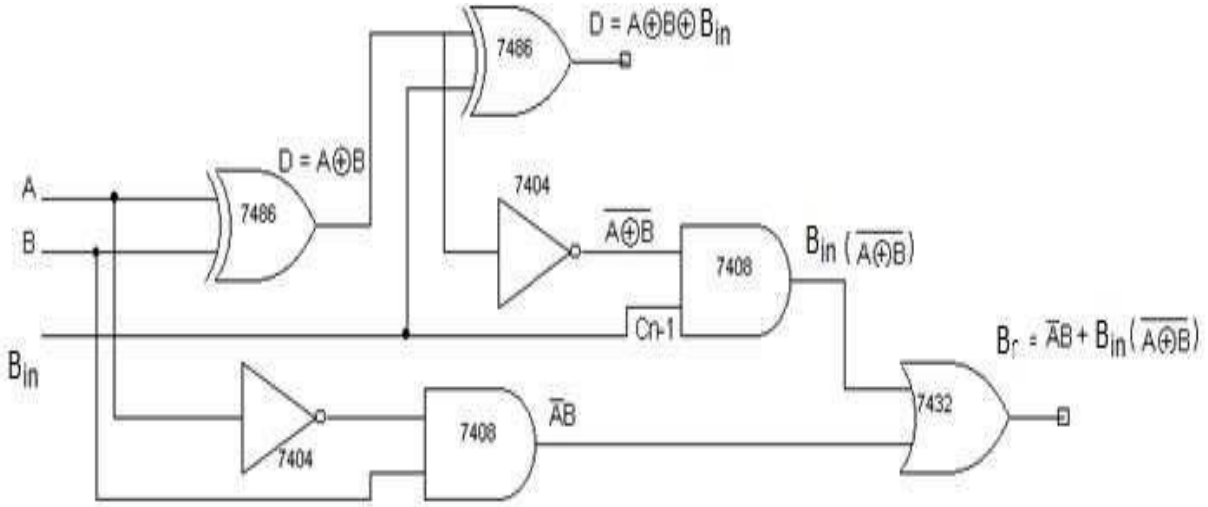
Procedure: -

1. Verify the gates.
2. Make the connections as per the circuit diagram.
3. Switch on V_{CC} and apply various combinations of input according to the truth table.
4. Note down the output readings for half and full subtractor difference and borrow bit for different combinations of inputs.

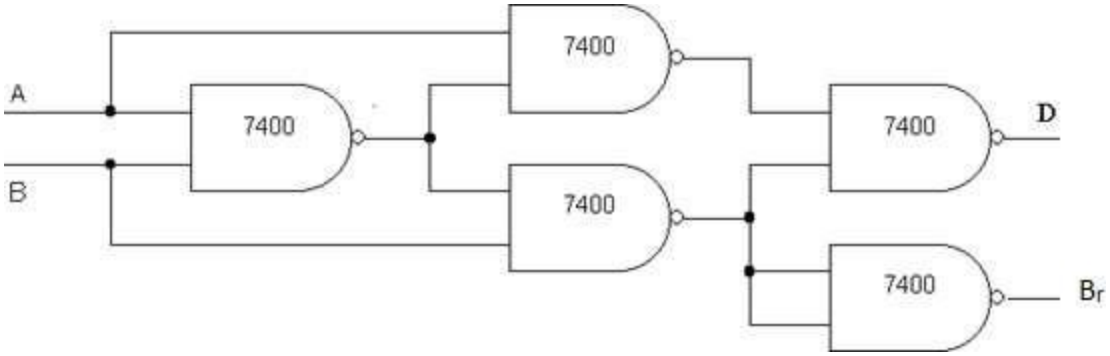
Using X – OR and Basic Gates (a)Half Subtractor



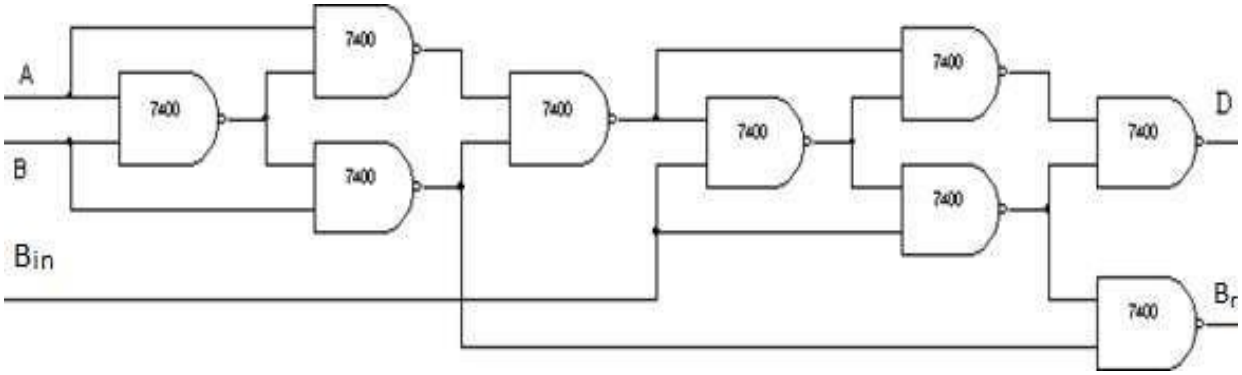
Full Subtractor



Using only NAND gate (a) Half subtractor

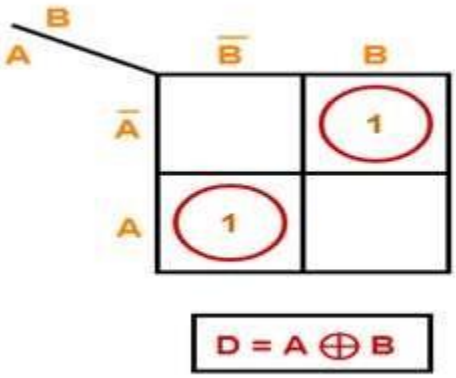


(b) Full Subtractor



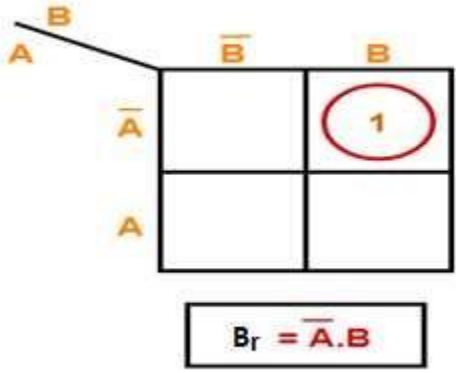
Half Subtractor			
A	**B**	**D**	**B_r**
0	0		
0	1		
1	0		
1	1		

For D:



$D = A \oplus B$

For B_r:

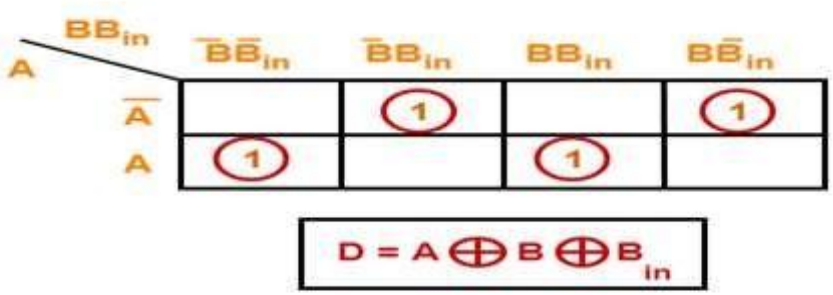


$B_r = \overline{A}.B$

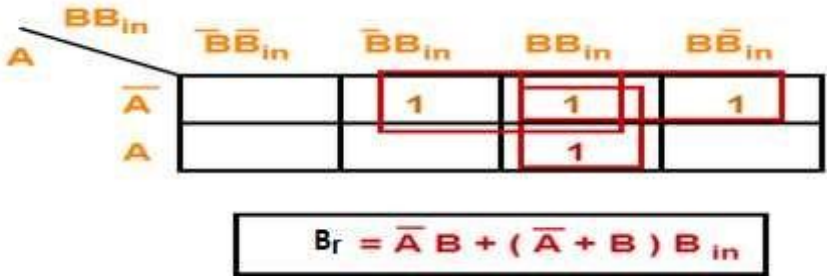
K Maps

Full Subtractor				
A	**B**	**B_{in}**	**D**	**B_r**
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

For D:



For B_r



Conclusion: -

Half subtractor and full subtractor are constructed and their truth tables are verified.

Experiment No:5 **Date:___/_/_**

Aim: - Implementation of a 4-bit Binary to Gray code converter.

APPARATUS REQUIRED

1. IC 7486
2. Digital trainer kit

THEORY:

Gray Code is one of the most important codes. It is a non-weighted code which belongs to aclass of codes called minimum change codes.

In this codes while traversing from one step to another step, only one bit in the code groupchanges.

The input variable are designated as B3, B2, B1, B0 and the output variables are designated asG3, G2, G1, G0.

Procedure: -

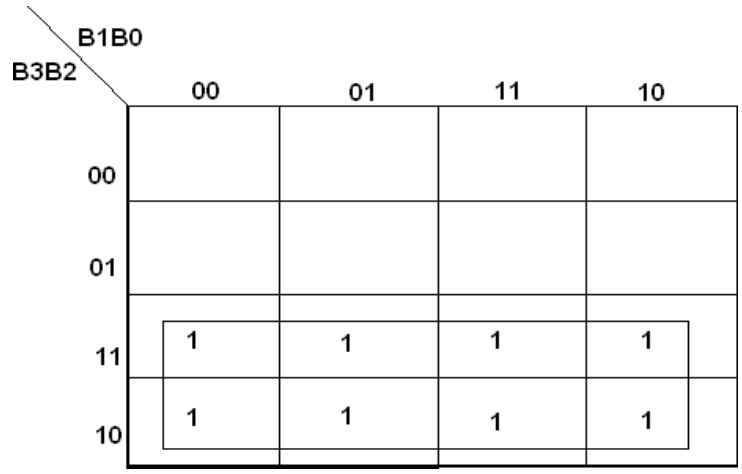
1. The circuit connections are made as shown in fig.
2. Pin (14) is connected to +Vcc and Pin (7) to ground.
3. In the case of binary to gray conversion, the inputs B0, B1, B2 and B3 are given at respective pins and outputs G0, G1, G2, G3 are taken for all the 16 combinations ofthe input.
4. The values of the outputs are tabulated.

TRUTH TABLE:

Binary Input					Gray code output			
B3	**B2**	**B1**	**B0**		**G3**	**G2**	**G1**	**G0**
0	**0**	**0**	**0**		**0**	**0**	**0**	**0**
0	**0**	**0**	**1**		**0**	**0**	**0**	**1**

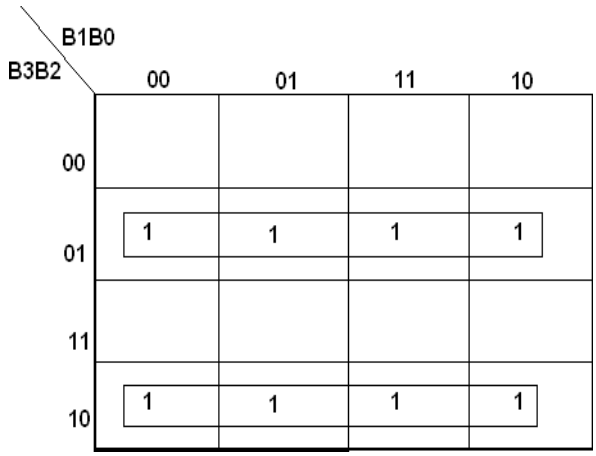
0	0	1	0		0	0	1	1
0	0	1	1		0	0	1	0
0	1	0	0		0	1	1	0
0	1	0	1		0	1	1	1
0	1	1	0		0	1	0	1
0	1	1	1		0	1	0	0
1	0	0	0		1	1	0	0
1	0	0	1		1	1	0	1
1	0	1	0		1	1	1	1
1	0	1	1		1	1	1	0
1	1	0	0		1	0	1	0
1	1	0	1		1	0	1	1
1	1	1	0		1	0	0	1
1	1	1	1		1	0	0	0

K-Map for G_3:



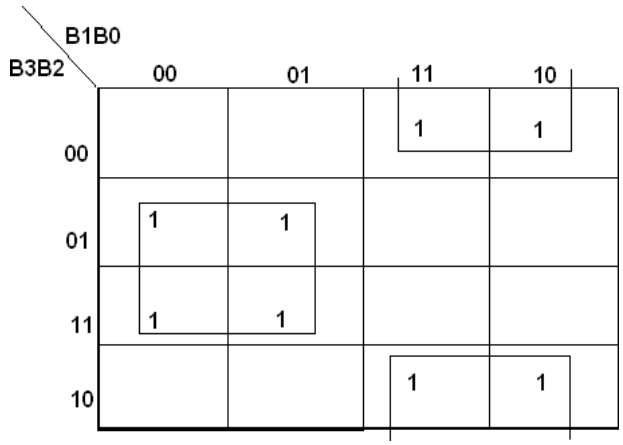
$G_3 = B_3$

K-Map for G_2:



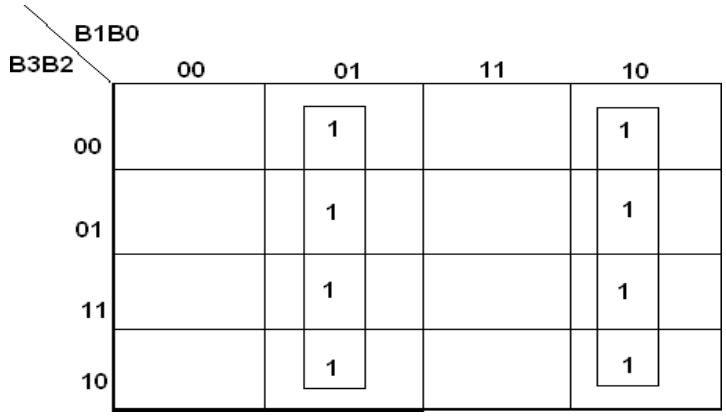
$G2 = B3 \oplus B2$

K-Map for G_1:



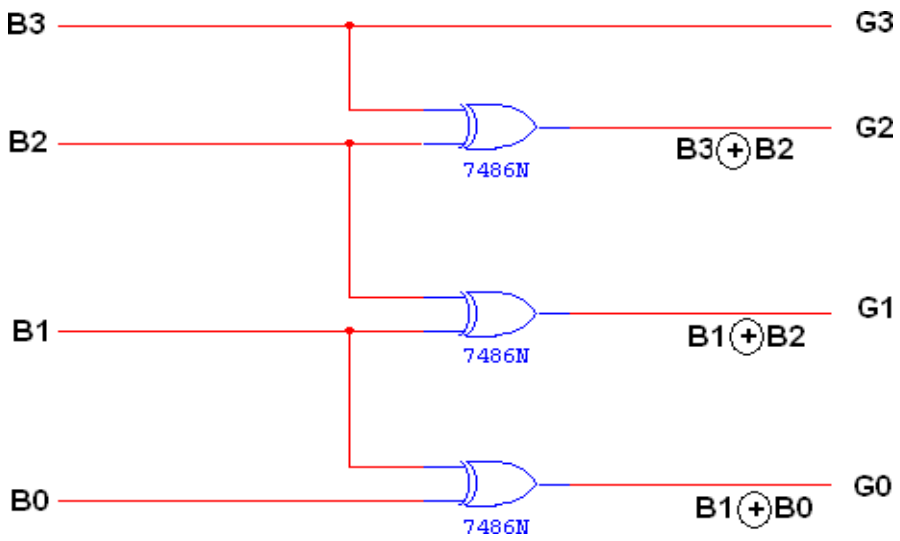
$G1 = B1 \oplus B2$

K-Map for G_0:



$G0 = B1 \oplus B0$

LOGIC DIAGRAM



Conclusion: -

4-bit Binary to Gray code converter is constructed and their truth tables are verified.

Experiment No:6 **Date:___/_/_**

Aim: - Implementation of a Single bit digital comparator.

APPARATUS REQUIRED

1. IC 7404,IC 7408,IC 74266
2. Digital trainer kit

THEORY:

Magnitude Comparator is a logical circuit, which compares two signals A and B and generatesthree logical outputs, whether A > B, A = B, or A < B.

Procedure: -

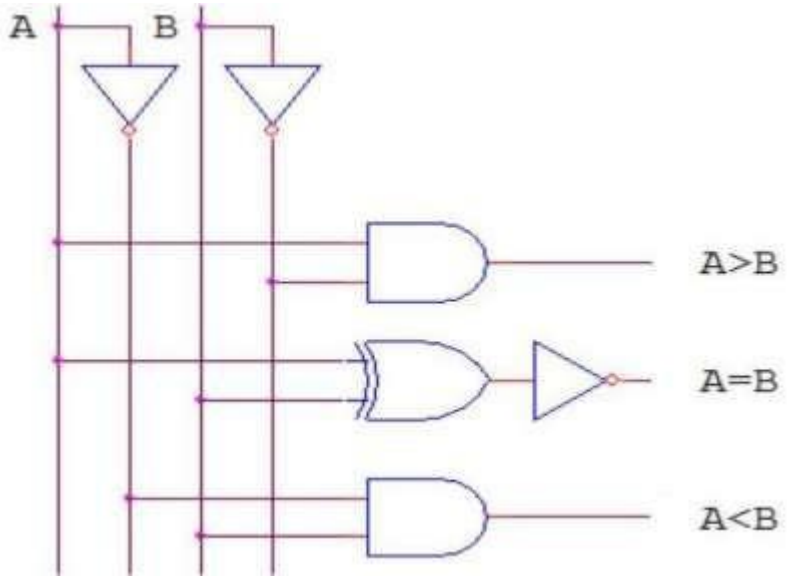
1. The circuit connections are made as shown in fig.
2. Pin (14) is connected to +Vcc and Pin (7) to ground.
3. The inputs A,B are given at respective pins and outputs A > B, A = B, or A < B are connected to the output LED.
4. The values of the outputs are tabulated.

$$A>B = A\overline{B}$$
$$A<B = \overline{A}B$$
$$A=B = \overline{A}\,\overline{B} + AB$$

TRUTH TABLE

INPUTS		OUTPUTS		
A	**B**	**A > B**	**A = B**	**A < B**
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

LOGIC DIAGRAM



Conclusion: -

A Single bit digital comparator is constructed and it's truth tables are verified.